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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/567,691	02/07/2006	Richard Petrus Kleihorst	NL 030972	3947

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
LAMARRE, GUY J	

ART UNIT	PAPER NUMBER
2112	

MAIL DATE	DELIVERY MODE
10/01/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/567,691	KLEIHORST ET AL.	
	Examiner	Art Unit	
	Guy J. Lamarre	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02/07/2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 February 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05/03/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

* **Claims 1-34** are rejected under 35 U.S.C. 102(b) as being anticipated by **KUO** (USPN 5940448, 8/17/99) -IDS of 05/03/2007- or in the alternative are rejected under 35 U.S.C. 103 (a) as being obvious over **KUO** and **Applicant's Admitted Prior Art** because **KUO's** deskewing methodology can be implemented in the traditional decoder at Fig. 1:*block 7* of the **Applicant's Admitted Prior Art .**

As per Claims 1-34, KUO discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM, an equivalent deskewing or phase compensating or phase error correcting methodology wherein data processing is delayed until phase compensation has taken place and data is stable enough for further processing, said deskewing comprising logic gates composed of latches/And-gates, …,. for delaying data flow through transmission lines/bus.

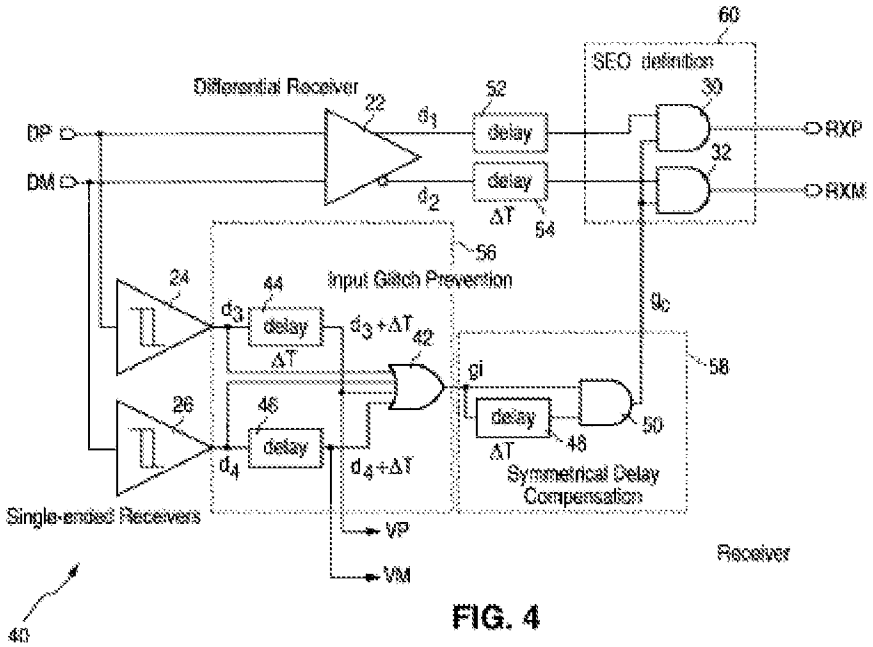

FIG. 4

As per Claims:

1, **KUO** discloses, e.g., in Fig. 4:*DP/DM/Blocks 56,58,60/RXP/RXM* - Fig. 5 and related description, an equivalent decoder circuit for a communication bus, the decoder circuit receiving a plurality of data signals from the communication bus, the data signals being susceptible of

being received at different times, wherein the decoder circuit comprises: a correction circuit for correcting one or more of the input signals; a control signal for controlling the correction circuit; a gating circuit, the gating circuit arranged in the path of the control signal; and a gating-Fig. 4:Block 48- control signal for controlling the gating circuit such that the control signal for controlling the correction circuit is blocked until a predetermined time.

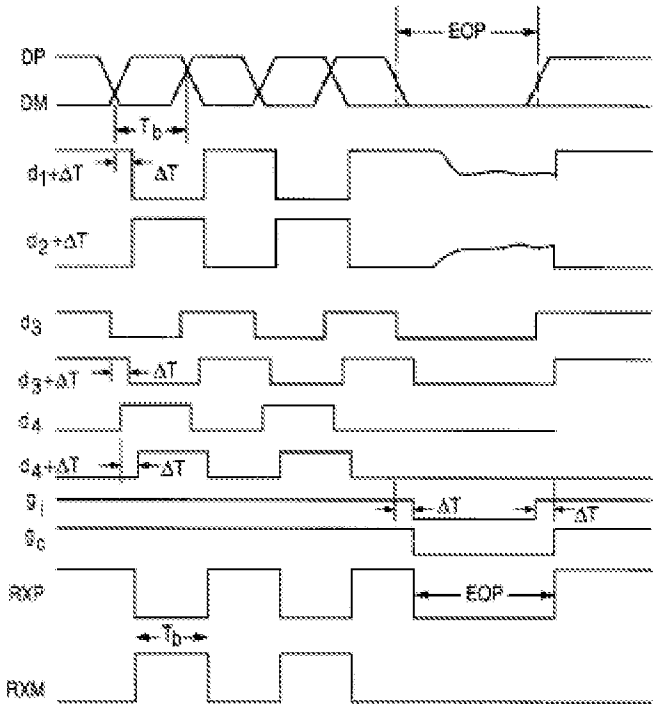

FIG. 5

2, **KUO** discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM - Fig. 5 and related description, an equivalent decoder-Fig. 1:Block 7 of Admitted Prior Art - circuit as claimed in claim 1, further comprising a parity circuit for generating a parity signal using the input data signals, the parity signal being used to generate said control signal for controlling the correction circuit.

3, **KUO** discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM - Fig. 5 and related description, an equivalent decoder-Fig. 1:Block 7 of **Admitted Prior Art** - circuit as claimed in claim 2, wherein the correction circuit comprises a plurality of multiplexers, each multiplexer-col. 4 line 55 et seq.- receiving an input data signal, and a copy of the input data signal, from the communication bus; a comparison circuit for comparing the parity signal generated by the parity circuit with a parity signal received from the communication bus, the comparison circuit providing the control signal for controlling the plurality of multiplexers to output either the input data signal or the copy of the input data signal.

4, **KUO** discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM - Fig. 5 and related description, an equivalent decoder-Fig. 1:Block 7 of **Admitted Prior Art** - circuit as claimed in claim 3, wherein the gating-Fig. 4:Block 48- circuit is located in the path of the control circuit such that it receives the output of the comparison circuit, and provides the control signal for controlling the plurality of multiplexers.

5, **KUO** discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM - Fig. 5 and related description, an equivalent decoder-Fig. 1:Block 7 of **Admitted Prior Art** - circuit as claimed in claim 2, further comprising a gating-Fig. 4:Block 48- circuit provided in the path of each input data signal and each copy of the input data signal, and wherein the plurality of gating-Fig. 4:Block 48- circuits are controlled by the gating control signal.

6, **KUO** discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM - Fig. 5 and related description, an equivalent decoder-Fig. 1:Block 7 of **Admitted Prior Art** - circuit as claimed in claim 3, further comprising a gating-Fig. 4:Block 48- circuit provided in the output path of

each multiplexer, and wherein the plurality of gating circuits are controlled by the gating control signal.

7, **KUO** discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM - Fig. 5 and related description, an equivalent decoder-Fig. 1:Block 7 of **Admitted Prior Art** - as claimed in claim 2, wherein the decoder-Fig. 1:Block 7 of **Admitted Prior Art** - is a dual-rail decoder.

8, **KUO** discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM - Fig. 5 and related description, an equivalent decoder-Fig. 1:Block 7 of **Admitted Prior Art** - circuit as claimed in claim 1, further comprising: a plurality of parity circuits, the parity circuits generating a plurality of parity signals from the input data signals; means for generating a plurality of control signals using the parity signals, the control signals being used to control the correction circuit; wherein a gating-Fig. 4:Block 48- circuit is provided in the path between each parity signal and the means for generating the plurality of control signals.

9, **KUO** discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM - Fig. 5 and related description, an equivalent decoder-Fig. 1:Block 7 of **Admitted Prior Art** - circuit as claimed in claim 8, wherein the correction circuit comprises a plurality of XOR gates, each XOR gate receiving an input data signal from the communication bus, and a control signal from the means for generating control signals.

10, **KUO** discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM - Fig. 5 and related description, an equivalent decoder-Fig. 1:Block 7 of **Admitted Prior Art** - circuit as claimed in claim 9, wherein the means for generating control signals is a syndrome decoder-Fig. 1:Block

7 of **Admitted Prior Art** - .

11, **KUO** discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM - Fig. 5 and related description, an equivalent decoder-Fig. 1:Block 7 of **Admitted Prior Art** - circuit as claimed in claim 8, wherein the decoder-Fig. 1:Block 7 of **Admitted Prior Art** - is a hamming decoder-Fig. 1:Block 7 of **Admitted Prior Art** - .

12, **KUO** discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM - Fig. 5 and related description, an equivalent decoder-Fig. 1:Block 7 of **Admitted Prior Art** - circuit as claimed in claim 1, wherein the gating-Fig. 4:Block 48- control signal is arranged to block the or each control signal from passing to the correction circuit until one or more of the input data signals have become stable.

13, **KUO** discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM - Fig. 5 and related description, an equivalent decoder-Fig. 1:Block 7 of **Admitted Prior Art** - circuit as claimed in claim 1, wherein the gating-Fig. 4:Block 48- control signal is arranged to block the or each control signal from passing to the correction circuit until all of the input data signals have become stable.

14, **KUO** discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM - Fig. 5 and related description, an equivalent decoder-Fig. 1:Block 7 of **Admitted Prior Art** - circuit as claimed in claim 1, wherein the gating-Fig. 4:Block 48- control signal is a delayed version of a system clock signal.

15, **KUO** discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM - Fig. 5 and related description, an equivalent decoder-Fig. 1:Block 7 of **Admitted Prior Art** - circuit as claimed in claim 1, wherein the gating-Fig. 4:Block 48- control signal is generated from the input data and/or parity bits.

16, **KUO** discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM - Fig. 5 and related description, an equivalent decoder-Fig. 1:Block 7 of **Admitted Prior Art** - circuit as claimed in claim 1, wherein the gating-Fig. 4:Block 48- circuit is an AND gate.

17, **KUO** discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM - Fig. 5 and related description, an equivalent decoder-Fig. 1:Block 7 of **Admitted Prior Art** - circuit as claimed in claim 1, wherein the gating-Fig. 4:Block 48- circuit is a latch.

18, **KUO** discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM - Fig. 5 and related description, an equivalent method of reducing power consumption in a decoder-Fig. 1:Block 7 of **Admitted Prior Art** - circuit for a communication bus, the decoder-Fig. 1:Block 7 of **Admitted Prior Art** - circuit receiving a plurality of data signals from the communication bus, the data signals being susceptible of being received at different times, wherein the decoder-Fig. 1:Block 7 of **Admitted Prior Art** - circuit comprises a correction circuit for correcting one or more of the input signals and a control signal for controlling the correction circuit, wherein the method comprises the steps of providing a gating-Fig. 4:Block 48- circuit in the path of the control signal, and controlling the gating circuit with a gating control signal, such that the control signal for controlling the correction circuit is blocked until a predetermined time.

19, **KUO** discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM - Fig. 5 and related description, an equivalent method as claimed in claim 18, wherein a parity circuit is provided for generating a parity signal using the input data signals, the parity signal being used to generate said control signal for controlling the correction circuit.

20, **KUO** discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM - Fig. 5 and related description, an equivalent method as claimed in claim 19, wherein the correction circuit comprises a plurality of multiplexers, each multiplexer-col. 4 line 55 et seq.- receiving an input data signal, and a copy of the input data signal, from the communication bus, and a comparison circuit for comparing the parity signal generated by the parity circuit with a parity signal received from the communication bus, the comparison circuit providing the control signal for controlling the plurality of multiplexers to output either the input data signal or the copy of the input data signal.

21, **KUO** discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM - Fig. 5 and related description, an equivalent method as claimed in claim 20, further comprising the step of locating the gating-Fig. 4:Block 48- circuit in the path of the control circuit such that it receives the output of the comparison circuit, and provides the control signal for controlling the plurality of multiplexers.

22, **KUO** discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM - Fig. 5 and related description, an equivalent method as claimed in claim 19 further comprising the step of providing a gating-Fig. 4:Block 48- circuit in the path of each input data signal and each copy of the input data signal, and controlling the plurality of gating-Fig. 4:Block 48- circuits with the

gating-Fig. 4:Block 48- control signal.

23, **KUO** discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM - Fig. 5 and related description, an equivalent method as claimed in claim 20, further comprising the step of providing a gating-Fig. 4:Block 48- circuit in the output path of each multiplexer, and controlling the plurality of gating circuits with the gating control signal.

24, **KUO** discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM - Fig. 5 and related description, an equivalent method as claimed in claim 19, wherein the decoder-Fig. 1:Block 7 of **Admitted Prior Art** - is a dual-rail decoder-Fig. 1:Block 7 of **Admitted Prior Art** - .

25, **KUO** discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM - Fig. 5 and related description, an equivalent method as claimed in claim 18, further comprising the steps of: providing a plurality of parity circuits, the parity circuits generating a plurality of parity signals from the input data signals; providing means for generating a plurality of control signals using the parity signals, the control signals being used to control the correction circuit; and providing a gating-Fig. 4:Block 48- circuit in the path between each parity signal and the means for generating the plurality of control signals.

26, **KUO** discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM - Fig. 5 and related description, an equivalent method as claimed in claim 25, wherein the correction circuit comprises a plurality of XOR gates, each XOR gate receiving an input data signal from the communication bus, and a control signal from the means for generating control signals.

27, **KUO** discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM - Fig. 5 and related description, an equivalent method as claimed in claim 26, wherein the means for generating control signals is a syndrome decoder-Fig. 1:Block 7 of **Admitted Prior Art** - .

28, **KUO** discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM - Fig. 5 and related description, an equivalent method as claimed in claim 25, wherein the decoder-Fig. 1:Block 7 of **Admitted Prior Art** - is a hamming decoder-Fig. 1:Block 7 of **Admitted Prior Art** - .

29, **KUO** discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM - Fig. 5 and related description, an equivalent method as claimed in claim 18, wherein the gating-Fig. 4:Block 48-control signal is arranged to block the or each control signal from passing to the correction circuit until one or more of the input data signals have become stable.

30, **KUO** discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM - Fig. 5 and related description, an equivalent method as claimed in claim 18, wherein the gating-Fig. 4:Block 48-control signal is arranged to block the or each control signal from passing to the correction circuit until all of the input data signals have become stable.

31, **KUO** discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM - Fig. 5 and related description, an equivalent method as claimed in claim 18, wherein the gating-Fig. 4:Block 48-control signal is a delayed version of a system clock signal.

32, **KUO** discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM - Fig. 5 and related description, an equivalent method as claimed in claim 18, wherein the gating-Fig. 4:Block 48-

control signal is generated from the input data and/or parity bits.

33, **KUO** discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM - Fig. 5 and related description, an equivalent method as claimed in claim 18, wherein the gating-Fig. 4:Block 48-circuit is an AND gate.

34, **KUO** discloses, e.g., in Fig. 4:DP/DM/Blocks 56,58,60/RXP/RXM - Fig. 5 and related description, an equivalent method as claimed in claim 18, wherein the gating-Fig. 4:Block 48-circuit is a latch.

Drawings

* The Drawings are objected to because Figures 1-6, referred to as conventional in the specification on page 5 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

CONCLUSION

* Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (571) 272-3826. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques, can be reached at (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Guy J Lamarre/
Primary Examiner, Art Unit 2112